A Scalable Model for the Substrate Resistance in Multi-Finger RF MOSFETs

Jeonghu Han and Hyungcheol Shin

Department of Electrical Engineering and Computer Science,
Korea Advanced Institute of Science and Technology (KAIST),
Guseong-dong, Yuseong-gu, Daejeon, 305-701, Korea

***Abstract* — We present a method to extract the substrate resistance of RF MOSFETs. We also analyze the substrate networks of multi-finger RF MOSFETs with vertical body contacts and propose a new method to predict the substrate resistance for any number of gate fingers. After the resistance components of the substrate networks are extracted, the effective substrate resistance is expressed as a function of the number of gate fingers. We compare the values of the substrate resistance predicted by the proposed method and extracted from *Y*-parameter data. The *Y*-parameters are obtained from both device simulation and measurement. The model predicts the substrate resistances accurately for multi-finger transistors.**

I. Introduction

The substrate resistance, R_{sub}, significantly affects the small-signal output characteristics of RF MOSFETs at high frequencies [1]-[5]. Recent RF MOSFET models include the substrate-related components, such as the junction capacitance and the substrate resistance. Accurate modeling of the substrate resistance is crucial for RF MOSFET modeling. A simple model consisting of a single resistance has been shown to be accurate up to 10 GHz [6]. We have suggested a method of extracting R_{sub} in [7].

The prediction of R_{sub} as a function of the number of gate fingers, N_f, is also important for the scalable model. It has been reported that R_{sub} is almost constant for devices with different N_f when N_f is a large number [8], [9]. However, the trends of R_{sub} predicted with the model in [8] and [9] were different from those of our measurement. We believe that's because the effect of the substrate resistances between junctions were neglected and therefore only the resistances from the transistor edges to the body contacts were considered for large N_f in [8]. In this paper, we proposed a new method to predict R_{sub} as a function of N_f. We have found that the resistances between junctions are considerable parts of the substrate resistance, especially when N_f is a large number. The prediction of R_{sub} was verified by comparing with R_{sub} extracted from Y-parameters of multi-finger transistors. We presented the results for both measurement and device simulation. It is shown that the new method predicts the R_{sub} very well.

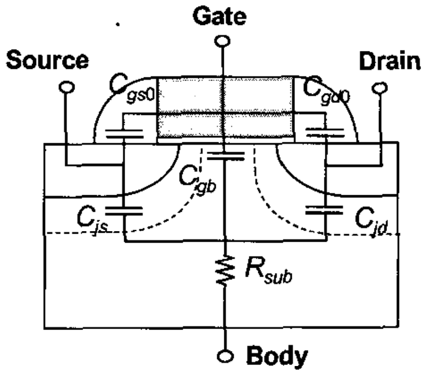


Fig. 1. Equivalent circuit of an RF MOSFET using a single substrate resistance, R_{sub}, when the device is turned off and the intrinsic components of the MOSFET are negligible.

II. Extraction Method of R_{SUB}

When the gate voltage is smaller than the threshold voltage, the intrinsic components of the device are negligible and the equivalent circuit is simplified as shown in Fig. 1 [7]. C_{gs0} and C_{gd0} represent the gate-to-source and the gate-to-drain zero-bias capacitances, respectively. C_{gb} indicates the sum of intrinsic and extrinsic gate-to-body capacitances. C_{js} and C_{jd} are source/drain junction capacitances. R_{sub} represents the substrate resistance. Through Y-parameter analysis, the elements in Fig. 1 can be represented by the following relationships:

$$C_{gd0} \approx -\frac{\mathrm{Im}[Y_{12}]}{\omega} \quad (1)$$

$$C_{gb} \approx \frac{\mathrm{Im}[Y_{11}]+2\,\mathrm{Im}[Y_{12}]}{\omega} \quad (2)$$

$$C_{jd} \approx \frac{\mathrm{Im}[Y_{22}]+\mathrm{Im}[Y_{12}]}{\omega} \quad (3)$$

$$R_{sub} \approx \frac{\mathrm{Re}[Y_{22}]}{(\mathrm{Im}[Y_{22}]+\mathrm{Im}[Y_{12}])^2} \quad (4)$$

0-7803-7695-1/03/$17.00 © 2003 IEEE

2003 IEEE MTT-S Digest

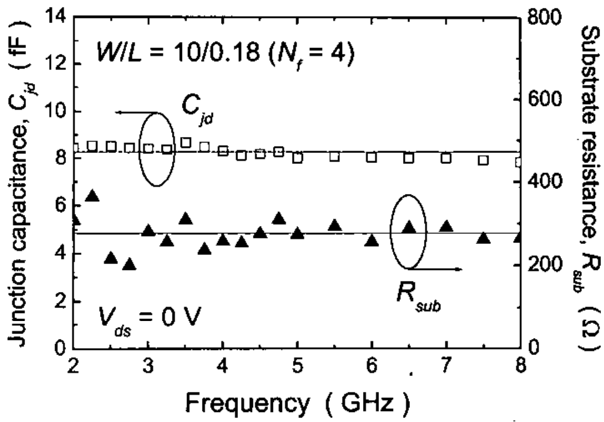


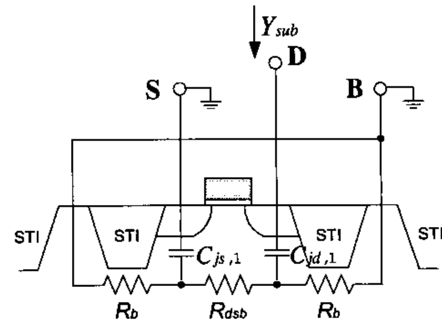
Fig. 2. C_{jd} and R_{sub} extracted from the measured Y-parameters of an RF MOSFET.

at frequencies up to a few GHz. C_{jd} and R_{sub} can be extracted from the measured Y-parameters by using (1)-(4). Fig. 2 shows the extracted C_{jd} and R_{sub} as functions of the frequency for a MOSFET with W/L = 10/0.18 and 4 gate fingers. The results were independent of the frequency for less than 8 GHz, where the components are accurately extracted.

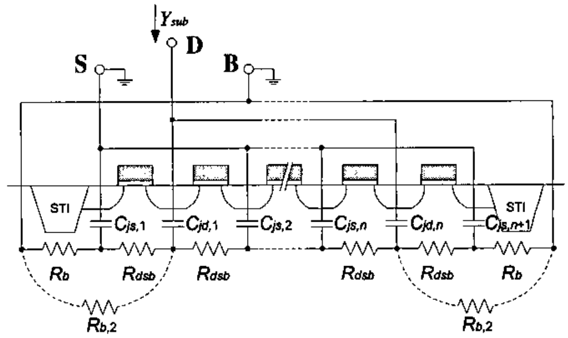
III. Analysis of the Substrate Network

The substrate networks were introduced to model the substrate resistance, R_{sub}, for multi-finger RF MOSFETs. Fig. 3 shows the cross sections and the substrate networks of multi-finger transistors when the body contacts are located at both sides of the device [9]. R_b is the resistance between the outmost junction and the body contact. R_{dsb} is the resistance between two adjacent junctions. The resistances from the internal junctions to the body contact through the bulk substrate were not illustrated in Fig. 3, since the resistive path through R_{dsb} (high doped region) is a dominant path rather than through the bulk substrate. After each resistance component was extracted, we have found that even the resistance from the second outmost junction to the body contact, $R_{b,2}$, was 15 times larger than $(R_b + R_{dsb})$, so that it can be omitted from the substrate networks.

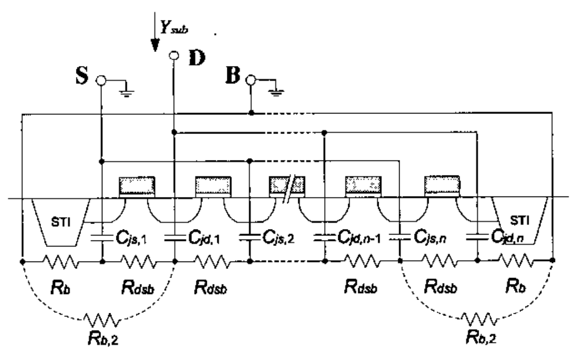
We derived the analytic equations for Y_{sub} of the substrate networks in Fig. 3 where the source and the body terminals are tied to ground. Y_{sub} is the admittance of the substrate networks to which only the substrate components contribute. Therefore, Y_{sub} can be considered as a series combination of C_{jd} and R_{sub} [10]. By analyzing the Y_{sub}, R_{sub} can be extracted as a function of R_b, R_{dsb}, and N_f. For a



(a) Single gate finger (N_f = 1)



(b) Even number of gate fingers ($N_f = 2n$)



(c) Odd number of gate fingers ($N_f = 2n-1$)

Fig. 3. Substrate networks for a single finger RF MOSFET and multi-finger RF MOSFETs.

single finger transistor shown in Fig. 3(a), R_{sub} is given by the following equation:

$$R_{sub} \approx \frac{R_b(R_b + R_{dsb})}{2R_b + R_{dsb}} \quad (5)$$

For multi-finger transistors shown in Fig. 3(b) and (c), R_{sub} are given by the following equations:

$$R_{sub} \approx \frac{R_b + R_{dsb}}{2} + \frac{R_{dsb}}{12}\frac{(N_f - 2)(N_f - 4)}{N_f} \quad (6)$$

for a device with an even number of fingers and

$$R_{sub} \approx \frac{R_b}{2} + \frac{R_{dsb}}{4} + \frac{R_{dsb}}{12}\frac{(N_f - 1)(N_f - 3)}{(N_f + 1)} \quad (7)$$

for a device with an odd number of fingers, where the number of fingers is denoted by N_f. For any number of fingers, the total junction capacitance, C_{jd}, is obtained by summing the capacitance of all the drain junctions as the following equation:

$$C_{jd} = \sum_i C_{jd,i} \quad (8)$$

The resistance value obtained from (6) is larger than that from (7) for any two consecutive numbers of fingers — one is even and the other is odd. The inequality means that R_{sub} for a transistor with an even number of fingers ($2n$) is larger than that for a transistor with the successive odd number of fingers ($2n$+1), since the distance from the outmost drain junction to the body contact is closer for the device with an odd number of fingers. Equations (6) and (7) show that R_{sub} increases with N_f, while the equations in [8] claim that R_{sub} decreases with N_f and it is saturated for large N_f. This difference will be discussed in the following section.

By using (5)-(7), R_b and R_{dsb} can be extracted from the measured R_{sub} for two or more devices with different numbers of fingers. After R_b and R_{dsb} are extracted, R_{sub} can be represented as a function of the N_f only, which enables to predict the values of R_{sub} for any number of gate fingers.

IV. Measurement Results and Discussions

The MOSFETs were fabricated in a commercially available 0.18-μm CMOS technology. The S-parameters were measured by using an Agilent 8510C vector network analyzer and a CASCADE Summit probe station. Open and short dummy patterns were used to de-embed the pad parasitics. The body contacts were located at both sides of each device. The schematic layout of the device is shown in Fig. 4. N_f in each device was 1, 2, 3, 4, 5, 6, 7, 8, or 16. The width of the gate fingers was fixed at 2.5 μm.

The values of R_{sub} were extracted from the measured Y-parameters by the method proposed in this paper and they are presented in Fig. 5. R_{sub} for a transistor with an even number of fingers is larger than that for the transistor with the following odd number of fingers, which was expected in (6) and (7). Fig. 5 also shows that R_{sub} increases with N_f as predicted in (6) and (7). When a transistor has a large N_f, the resistances from the inner junctions to the body contacts increase. They make large contributions to the real part of Y_{sub}, so that the effective substrate resistance, R_{sub}, increases.

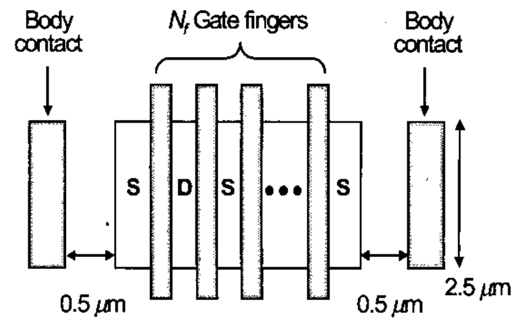


Fig. 4. Schematic layout of the device with substrate contacts.

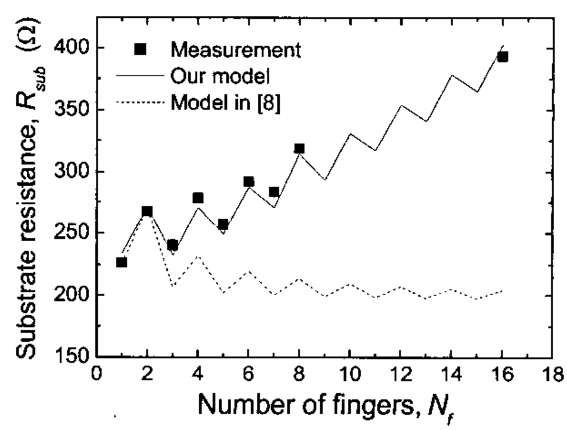


Fig. 5. The prediction of R_{sub} for the devices with multiple gate fingers.

From the measurement results, we extracted R_b and R_{dsb} of the substrate networks in Fig. 3. R_{dsb} was extracted from the slope of R_{sub} to N_f, since the slope is $R_{dsb}/12$ (see (6) and (7)). R_{dsb} was 151 Ω and R_b was calculated to be 389 Ω by using (5).

R_{sub} were predicted for N_f from 1 to 16 by using (5)-(7) and they are presented in Fig. 5. The prediction matches well with the extracted R_{sub}. For comparison, R_{sub} were also estimated from the relationships in [8]. The dotted lines in Fig. 5 show that the trends of R_{sub} estimated by the method in [8] slightly decrease with N_f, which cannot predict the measurement results correctly.

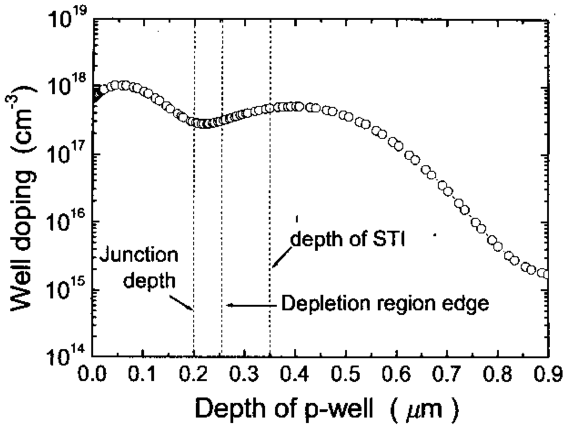


Fig. 6. Doping concentration of the p-well for the MOSFET structures created by the ATLAS device simulator.

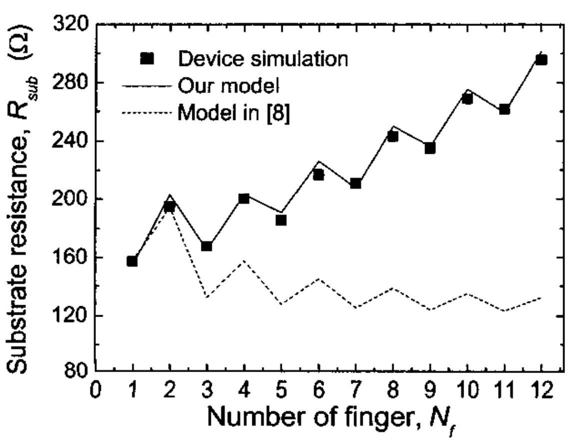


Fig. 7. The prediction of R_{sub} for the devices with multiple gate fingers, where the devices were created by the ATLAS device simulator.

V. Simulation Results

We also verified our model by performing the device simulation. The MOSFET structures were created with N_f varying from 1 to 12 by using the ATLAS device simulator. The width of the gate fingers was 10 μm. The body contacts were placed at both sides of the device as illustrated in Fig. 3. The doping profile of the p-well and some information on the device dimensions are presented in Fig. 6. The Y-parameters were obtained by executing the ac simulation.

The values of R_{sub} were extracted from the simulated Y-parameters and they are presented in Fig. 7. A very similar result to the measured one was observed. R_{sub} increased with N_f as expected.

VI. Conclusion

We proposed a method to extract the substrate resistance, R_{sub} of RF MOSFETs. We analyzed the substrate networks of multi-finger RF MOSFETs and derived analytic equations to predict R_{sub} as a function of the number of gate fingers, N_f. For a large N_f, the effect of internal resistance, R_{dsb}, is significant rather than negligible, so that the R_{sub} increased with N_f. The trends of R_{sub} were shown for the simulated and measured devices and were predicted accurately by the model proposed in this paper.

Acknowledgement

This work was supported in part by the National Program for Tera-level Nano Devices through MOST and by the System IC 2010 project. The authors also would like to thank Kwangseok Han and Minkyu Je for helpful discussions.

References

[1] J-J. Ou, X. Jin, I. Ma, C. Hu, and P. R. Gray, "CMOS RF modeling for GHz communication IC's," *1998 VLSI Technology Symp. Tech. Dig.*, pp. 94-95, 1998.

[2] S. H-M. Jen, C. C. Enz, D. R. Pehlke, M. Schröter, and B. J. Sheu, "Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz," *IEEE Trans. Electron Devices*, vol. 46, no. 11, pp. 2217-2227, Nov. 1999.

[3] R. Sung, P. Bendix, and M. B. Das, "Extraction of high-frequency equivalent circuit parameters of submicron gate-length MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, no. 8, pp. 1769-1775, Aug. 1998.

[4] L. Tiemeijer and D. Klaassen, "Geometry scaling of the substrate loss of RF MOSFETs," *28th Eur. Solid-State Device Research Conf. (ESSDERC) Tech. Dig.*, pp. 480-483, 1998.

[5] I. Kwon, M. Je, K. Lee, and H. Shin, "A simple and analytical parameter extraction method of MOSFET for microwave modeling," *IEEE Trans. Microwave Theory and Tech.*, vol. 50, no. 6, pp. 1503-1509, June 2002.

[6] S. F. Tin, A. A. Osman, K. Mayaram, and C. Hu, "A simple subcircuit extension of the BSIM3v3 model for CMOS RF design," *IEEE Jour. Solid-State Circ.*, vol. 35, no. 4, pp. 612-624, Apr. 2000.

[7] J. Han, M. Je, and H. Shin, "A simple and accurate method for extracting substrate resistance of RF MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 434-436, July 2002.

[8] Y. Cheng and M. Matloubian, "Parameter extraction of accurate and scaleable substrate resistance components in RF MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp.221-223, Apr. 2002.

[9] C. C. Enz and Y. Cheng, "MOS transistor modeling for RF IC design," *IEEE Jour. Solid-State Circ.*, vol. 35, no. 2, pp.186-201, Feb. 2000.

[10] Y. Cheng and M. Matloubian, "On the high-frequency characteristics of substrate resistance in RF MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 12, pp. 604-606, Dec. 2000.